FIG. 1

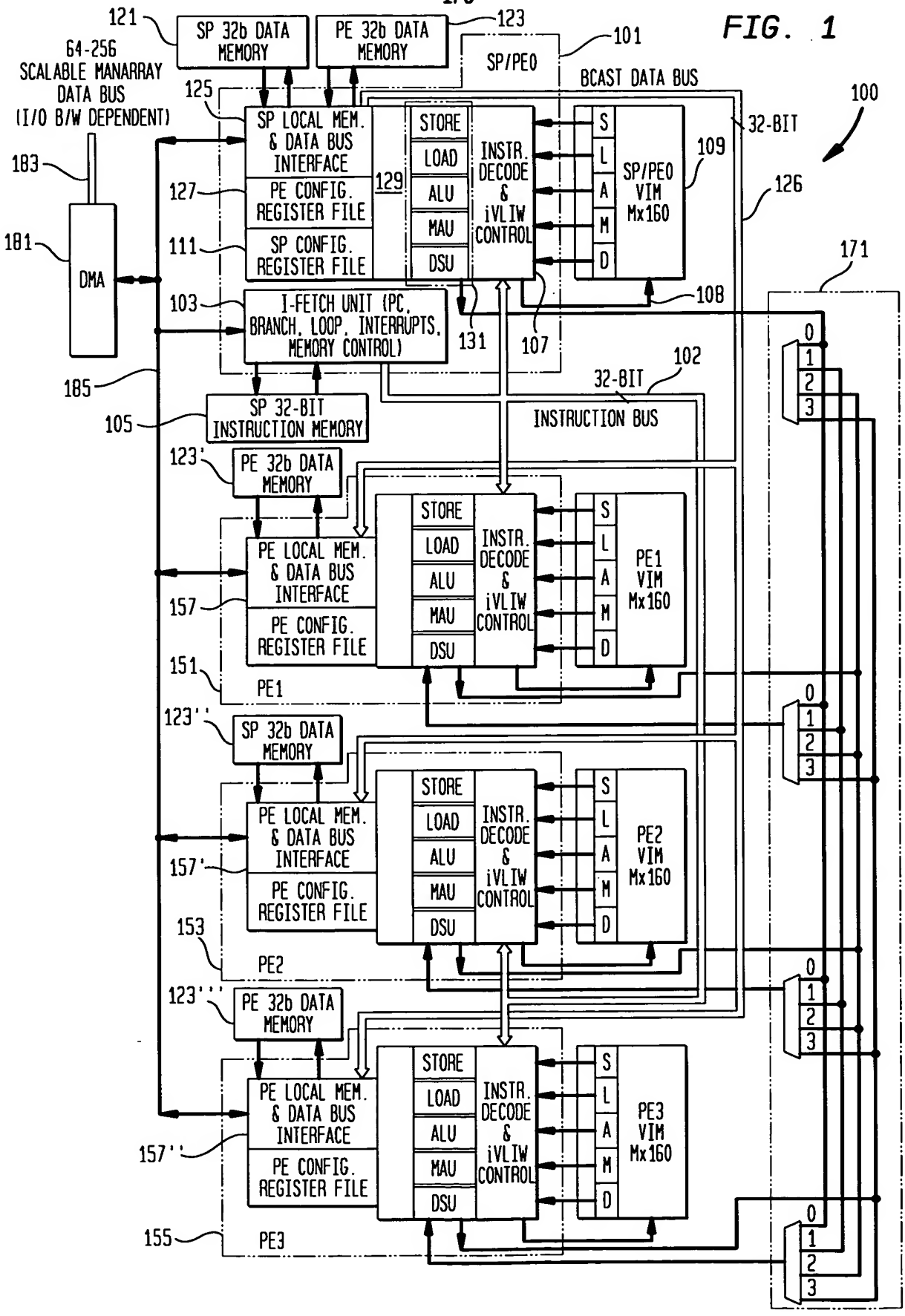

121
SP 32b DATA MEMORY
123
PE 32b DATA MEMORY
101
SP/PE0
BCAST DATA BUS
100
64-256 SCALABLE MANARRAY DATA BUS (I/O B/W DEPENDENT)
125
SP LOCAL MEM. & DATA BUS INTERFACE
PE CONFIG. REGISTER FILE
SP CONFIG. REGISTER FILE
129
STORE
LOAD
ALU
MAU
DSU
INSTR. DECODE & iVLIW CONTROL
S
L
A
M
D
SP/PE0 VIM Mx160
109
32-BIT
126
171
183
181
DMA
127
111
103
I-FETCH UNIT (PC, BRANCH, LOOP, INTERRUPTS, MEMORY CONTROL)
131
107
108
185
105
SP 32-BIT INSTRUCTION MEMORY
102
32-BIT
INSTRUCTION BUS
123'
PE 32b DATA MEMORY
PE LOCAL MEM. & DATA BUS INTERFACE
PE CONFIG. REGISTER FILE
157
PE1 VIM Mx160
151
PE1
123''
SP 32b DATA MEMORY
157'
PE2 VIM Mx160
153
PE2
123'''
PE 32b DATA MEMORY
157''
PE3 VIM Mx160
155
PE3
0
1
2
3

FIG. 2A

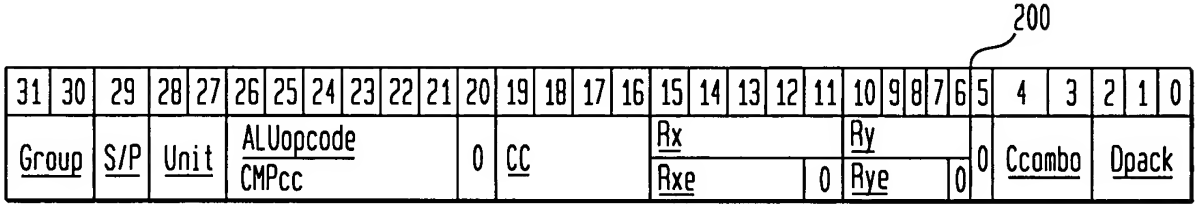


FIG. 2B

202

	CC	Description	C-N-V-Z Setting
204	Z(EQ)	Zero or Equal	Z=1
	NZ(NE)	Not Zero or Not Equal	Z=0
	HI	Higher (unsigned)	(C=1)&&(Z=0)
	HS(CS)	Higher or Same (unsigned, or Carry Set)	C=1
	LO(CC)	Lower (unsigned, or Carry Clear)	C=0
	LS	Lower or Same (unsigned)	(C=0) || (Z=1)
	VS	Overflow Set	V=1
	VC	Overflow Clear	V=0
	POS	Positive	(N=0)&&(Z=0)
	NEG	Negative	N=1
205	GE	Greater-than or Equal (signed)	N=V
206	GT	Greater-Than (signed)	(Z=0)&&(N=V)
207	LE	Less-than or Equal (signed)	(Z=1) || (N!=V)
208	LT	Less-Than (signed)	N!=V

FIG. 3A

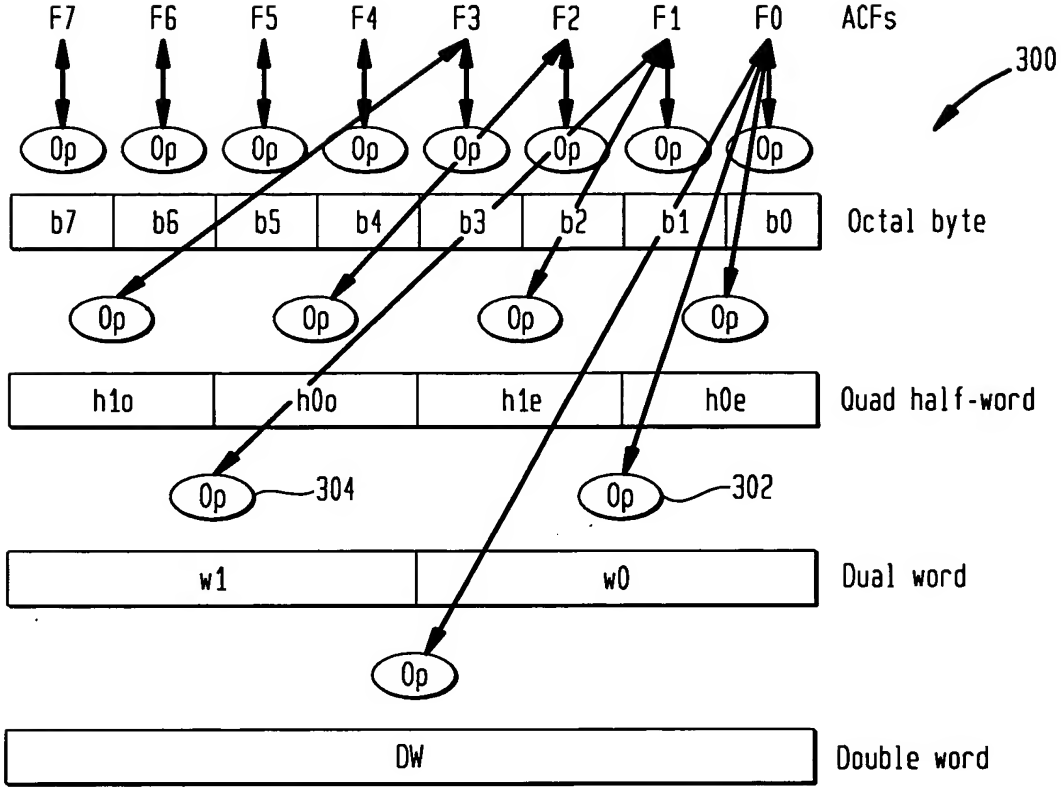

F7
F6
F5
F4
F3
F2
F1
F0
ACFs
300
Op
b7
b6
b5
b4
b3
b2
b1
b0
Octal byte
h1o
h0o
h1e
h0e
Quad half-word
304
302
w1
w0
Dual word
DW
Double word

FIG. 3B

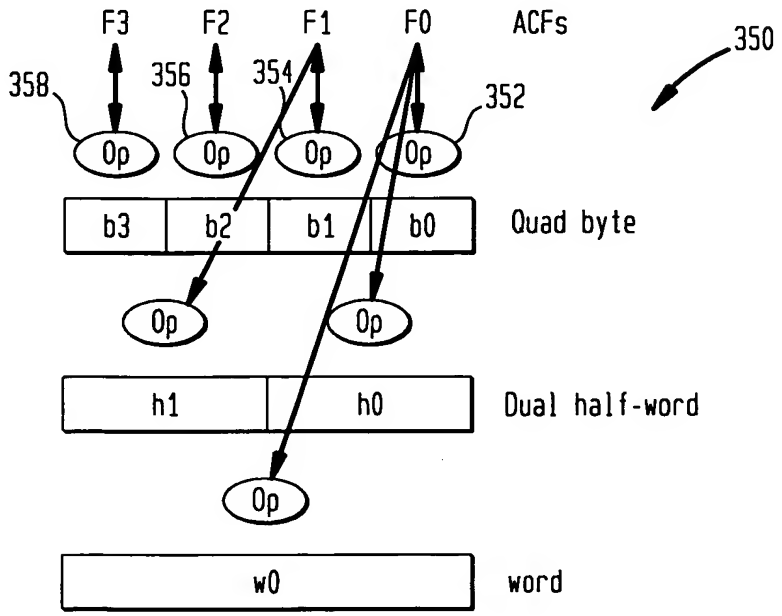

F3
F2
F1
F0
ACFs
350
358
356
354
352
Op
b3
b2
b1
b0
Quad byte
h1
h0
Dual half-word
w0
word

FIG. 4A

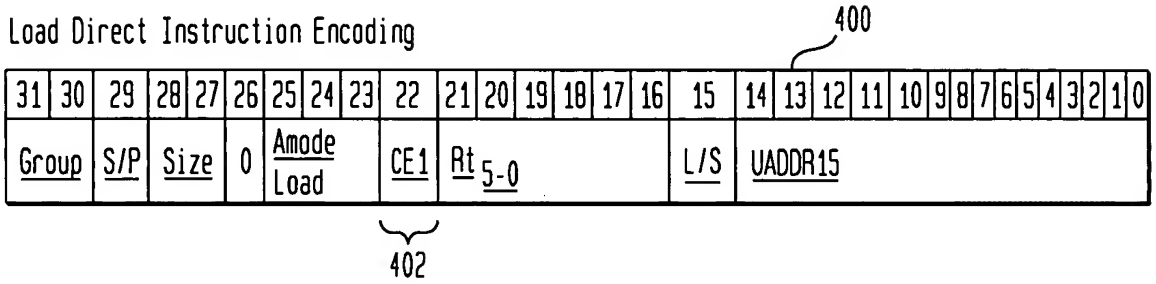


FIG. 4B

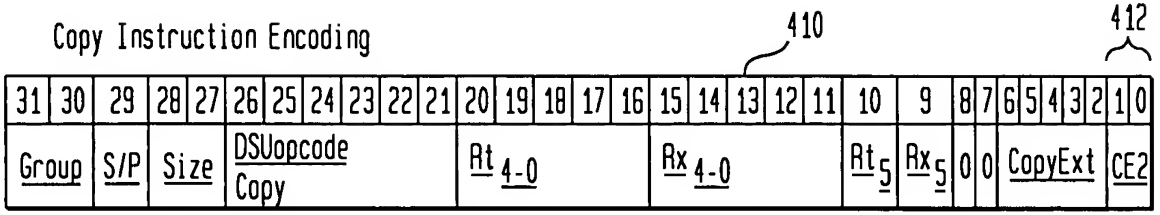


FIG. 4C

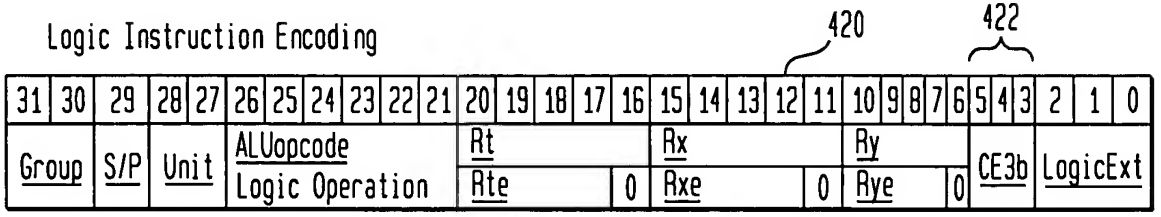
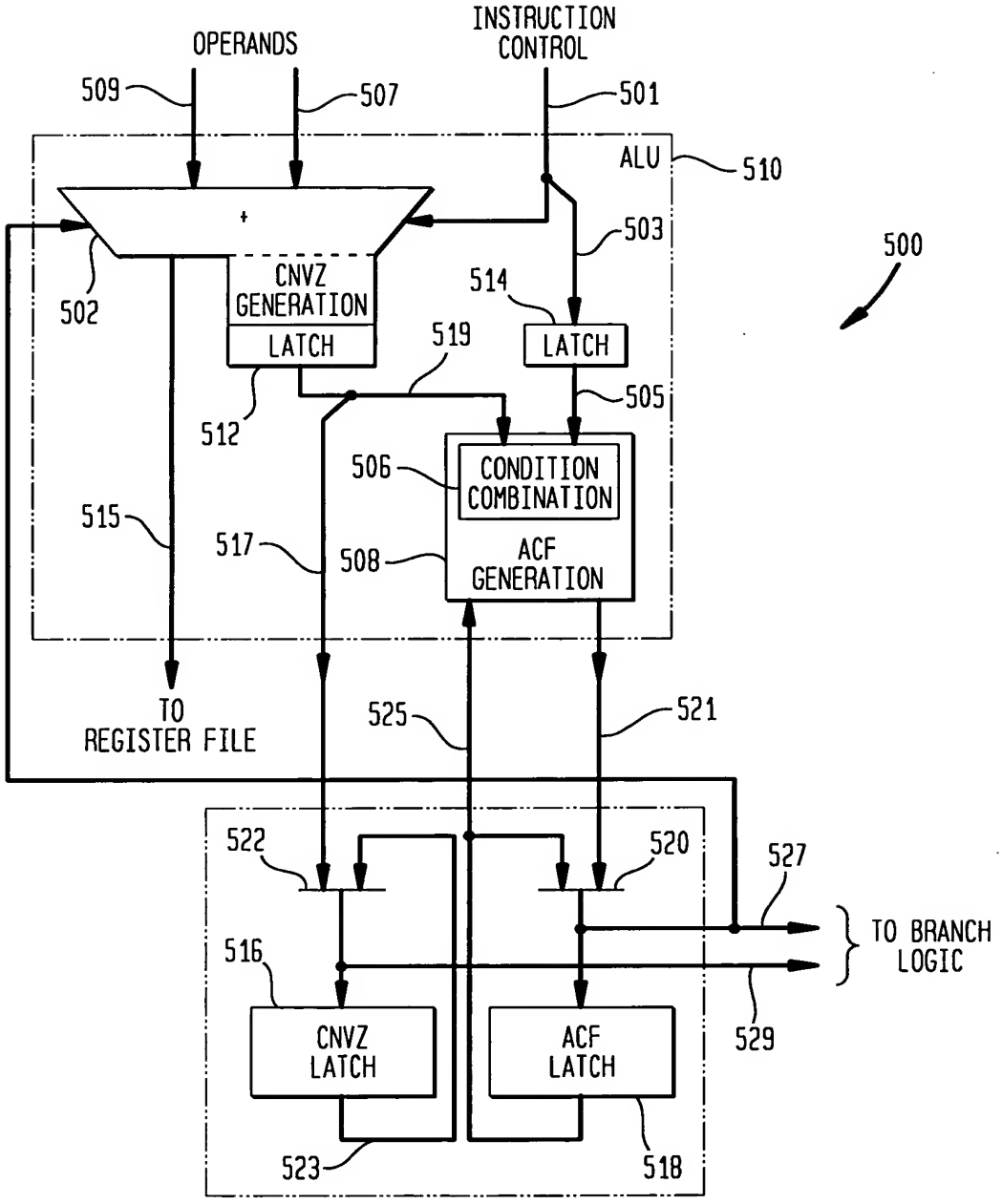


FIG. 5A


OPERANDS
INSTRUCTION CONTROL
509
507
501
ALU
510
+
503
500
502
CNVZ GENERATION
LATCH
514
LATCH
519
512
505
506
CONDITION COMBINATION
515
517
508
ACF GENERATION
TO REGISTER FILE
525
521
522
520
527
TO BRANCH LOGIC
516
CNVZ LATCH
ACF LATCH
529
523
518

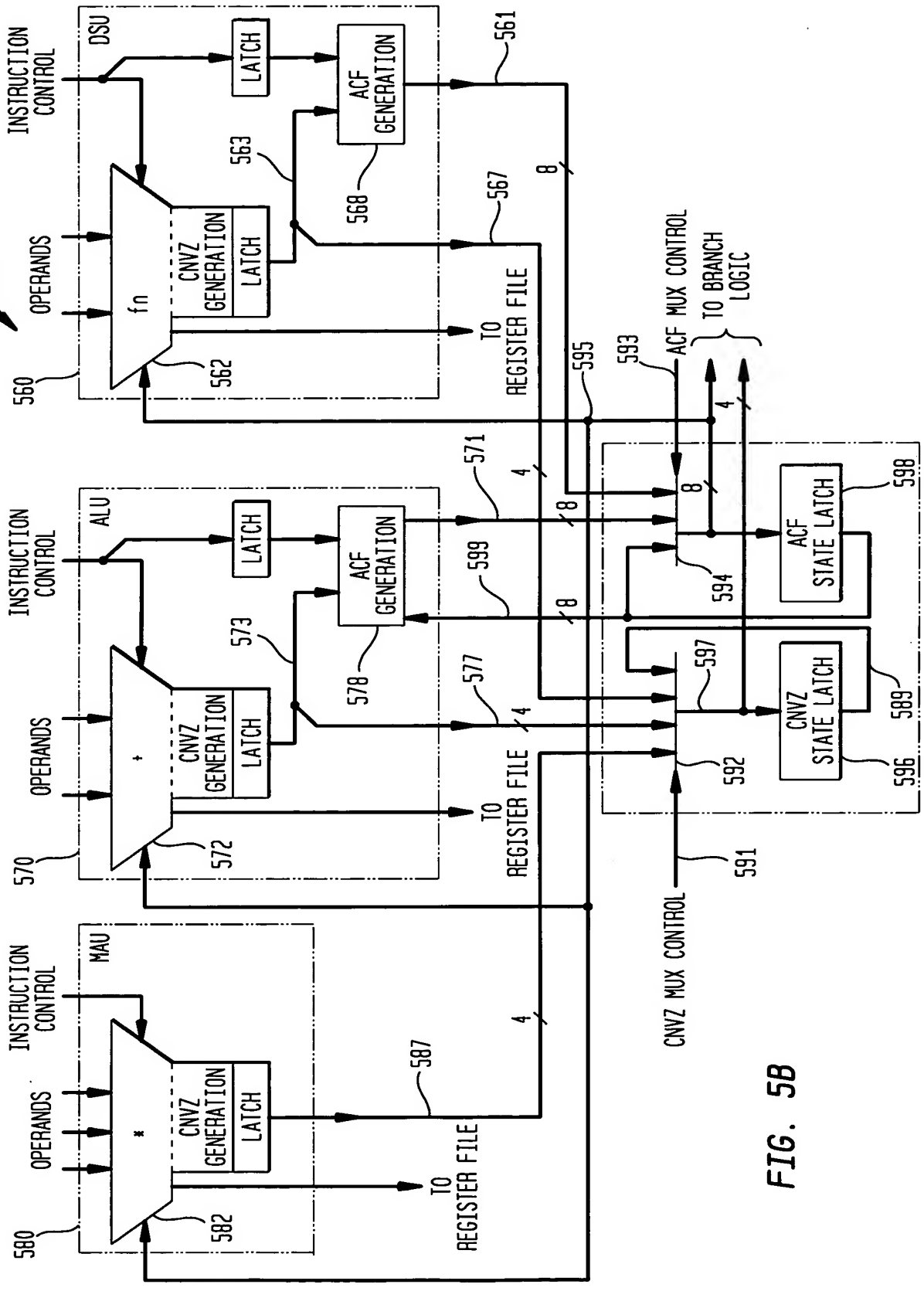

550
DSU
INSTRUCTION CONTROL
OPERANDS
fn
LATCH
CNVZ GENERATION
LATCH
ACF GENERATION
560
562
563
567
568
561
TO REGISTER FILE
ALU
INSTRUCTION CONTROL
OPERANDS
+
LATCH
CNVZ GENERATION
LATCH
ACF GENERATION
570
572
573
577
578
571
599
TO REGISTER FILE
MAU
INSTRUCTION CONTROL
OPERANDS
*
CNVZ GENERATION
LATCH
580
582
587
TO REGISTER FILE
595
593
ACF MUX CONTROL
TO BRANCH LOGIC
CNVZ MUX CONTROL
591
592
594
597
ACF STATE LATCH
CNVZ STATE LATCH
598
589
596

FIG. 5B